

Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) EP 0 821 427 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
28.01.1998 Bulletin 1998/05

(51) Int. Cl.⁶: H01P 5/08

(21) Application number: 97112280.9

(22) Date of filing: 17.07.1997

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC
NL PT SE

(30) Priority: 26.07.1996 JP 197641/96

(71) Applicant:
MURATA MANUFACTURING CO., LTD.
Nagaokakyo-shi Kyoto-fu 226 (JP)

(72) Inventors:
• Ishikawa, Yohei
Nagaokakyo-shi, Kyoto-fu (JP)

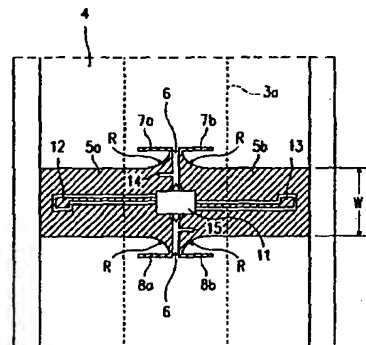
• Sakamoto, Koichi
Nagaokakyo-shi, Kyoto-fu (JP)
• Yamashita, Sadao
Nagaokakyo-shi, Kyoto-fu (JP)
• Kajikawa, Takehisa
Nagaokakyo-shi, Kyoto-fu (JP)

(74) Representative:
Schoppe, Fritz, Dipl.-Ing.
Patentanwalt,
Postfach 71 08 67
81458 München (DE)

(54) Dielectric line waveguide

(57) An amplifying circuit is formed by a combination of a dielectric line waveguide and a semiconductor device (11; 31; 34). Two electrically conductive plates (1, 2) are provided substantially parallel to each other. Two dielectric strips (3a, 3b) are disposed between the two conductive plates (1, 2), and a dielectric plate (4) is further inserted between the dielectric strips (3a, 3b). Ground conductors (5a, 5b) are formed on the dielectric plate (4). The ground conductors (5a, 5b) have an area which equals an amount required for blocking a RF signal propagating in the dielectric line waveguide. A slot line (6) is formed between the ground conductors (5a, 5b) in a position corresponding to the inside of the dielectric strips (3a, 3b). Line-switching conductor patterns (7a, 7b, 8a, 8b) are provided at both sides of the ends of the slot line. A field-effect transistor (11) is mounted on the slot line (6) such that it bridges over the slot line (6). Accordingly, losses and distortion of an RF signal, which would occur in an input/output circuit, are suppressed, and the generation of parasitic coupling is eliminated. Further, the dielectric line waveguide is miniaturized free from an external circuit, and accordingly, the manufacturing cost is reduced as well.

FIG. 1 (A)



Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a dielectric line waveguide which forms an amplifying circuit or a modulation circuit, used in, for example, a circuit module in a millimetric wave or microwave band.

2. Description of the Related Art

Hitherto, a dielectric line waveguide is used as a communication module in a millimetric wave band. In particular, a nonradiative dielectric line waveguide (NRD guide) is free from radiation losses and can be miniaturized due to its configuration such that a dielectric strip is inserted between two plane-parallel plates having an interval of a half-wave length or less. Thus, research is being made on applications of the NRD guides to millimetric-wave integrated circuits. An example of applications of the above type of dielectric line waveguide to an amplifying circuit is shown in *HEMT Amplifier Used in NRD Guide Integrated Circuit*, by Wilkinson, A. A, and Tsutomu Yoneyama, The 1990 IEICE Spring Conference, SC-2-2, (1990) pp. 2-627.

In an amplifying circuit formed by a combination of a dielectric line waveguide and a semiconductor device, as shown in the above example, the semiconductor device is conventionally disposed outside the dielectric line waveguide. Accordingly, a signal propagating in the dielectric line waveguide is first output from the waveguide and is then processed in the semiconductor device, and is once again returned to the dielectric line waveguide.

When a frequency signal (RF signal) is input into or output from a semiconductor device, impedance matching should be, in general, performed in an input/output circuit provided between a transmission line and the semiconductor device in order to improve input/output efficiency. However, the foregoing amplifying circuit in which the semiconductor device is provided on the exterior of the dielectric line waveguide encounters the following problems. Loss and distortion may be incurred in the RF signal while impedance matching is performed in the input/output circuit, such as a matching circuit, and parasitic coupling is easily generated between an external circuit, such as a semiconductor device, and the dielectric line waveguide, thereby degrading the RF characteristics. Further, the configuration of the circuit is complicated, which inevitably makes the manufacturing process very complicated as well.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a dielectric line waveguide free from the

above-described problems, such as loss and distortion incurred in RF signals in an input/output circuit, and parasitic coupling generated between an external circuit and the dielectric line waveguide, in which miniaturization of the dielectric line waveguide can be enhanced free from external circuits, and the manufacturing cost can be reduced accordingly.

In order to achieve the above object, according to the present invention, there is provided a dielectric line waveguide comprising: two electrically conductive plates disposed substantially parallel to each other; a dielectric strip disposed between the two electrically conductive plates; a dielectric plate disposed between the two electrically conductive plates; a ground conductor formed on the dielectric plate and having an area which equals an amount required for blocking a frequency signal propagating in the dielectric line waveguide, the ground conductor having a slot line at a position corresponding to the inside of the dielectric strip; a line-switching conductor pattern provided for the ground conductor at a position corresponding to an end of the slot line, the conductor pattern being coupled to electromagnetic fields generated in the slot line and in the dielectric strip; and a semiconductor device disposed on the slot line in such a manner that it bridges over the slot line.

With this arrangement, a longitudinal section magnetic (LSM)-mode RF signal propagating in the dielectric strip is coupled to the line-switching conductor pattern and is converted into a TE-mode signal. The TE-mode signal further propagates in the slot line and is input into the semiconductor device. Conversely, a TE-mode signal output from the semiconductor device propagates in the slot line and is converted into a LSM-mode RF signal via the line-switching conductor pattern provided at an end of the slot line. The LSM-mode RF signal further propagates in the dielectric strip. Accordingly, a circuit formed of a semiconductor device is formed on the dielectric plate at a position corresponding to the inside of the dielectric strip. This eliminates the generation of parasitic coupling between the dielectric line waveguide and an external circuit, which would otherwise be caused if an external circuit is provided. Also, transmission losses generated at a connecting portion between the dielectric strip and the semiconductor device can be inhibited to a minimal level. Moreover, it is possible to fabricate the ground conductor and the line-switching conductor pattern on the dielectric plate according to a technique similar to the typical manufacturing method for a printed wiring board. The manufacturing cost can thus be reduced.

In the above dielectric line waveguide, the line-switching conductor patterns may be respectively provided in positions at both sides of an end of the slot line, and the semiconductor device may be disposed substantially at the center of the slot line. Thus, a frequency signal (RF signal) propagating in the dielectric line waveguide is interrupted in and by the action of the

ground conductor disposed on the dielectric plate. Accordingly, two dielectric lines are formed in a continuous dielectric strip, and are connected to each other via the semiconductor device. It is thus possible to readily construct a dielectric line waveguide provided with an amplifying circuit by using, for example, a FET.

Further, in the above dielectric line waveguide, a $\lambda/4$ short stub used for providing impedance matching between the line-switching conductor pattern and the semiconductor device may be provided in a midpoint of the slot line. This achieves impedance matching between the line-switching conductor pattern and the semiconductor device, thereby inhibiting transmission losses at a connecting portion between the slot line and the semiconductor device.

Additionally, in the above dielectric line waveguide, an impedance matching circuit may be provided between the line-switching conductor pattern and the slot line. This realizes the impedance matching between the slot line and the line-switching conductor pattern and between the slot line and the dielectric line waveguide. It is thus possible to suppress unwanted reflection, and inhibit transmission losses incident to a line-switching operation.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1, which is comprised of Figs. 1A and 1B, illustrates the configuration of a dielectric line waveguide provided with an oscillator circuit according to a first embodiment of the present invention;

Fig. 2, which is comprised of Figs. 2A and 2B, illustrates the configuration of a field-effect transistor (FET) and a dielectric plate on which the FET is mounted;

Fig. 3, which is comprised of Figs. 3A and 3B, illustrates a modification made to the line-switching conductor patterns shown in Fig. 1;

Fig. 4, which is comprised of Figs. 4A and 4B, illustrates the configuration of a dielectric line waveguide provided with a frequency-variable portion of a voltage-controlled oscillator according to a second embodiment of the present invention;

Fig. 5, which is comprised of Figs. 5A and 5B, illustrates the configuration of a dielectric line waveguide provided with a mixer circuit according to a third embodiment of the present invention;

Fig. 6, which is comprised of Figs. 6A and 6B, illustrates the configuration of the mixer diode shown in Fig. 5;

Fig. 7 illustrates the connecting relationship between the mixer diode and the pattern formed on the dielectric plate; and

Fig. 8, which is comprised of Figs. 8A, 8B and 8C, illustrates modifications made to the line-switching conductor patterns.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A description will now be given with reference to Figs. 1 through 3 of the configuration of a dielectric line waveguide provided with an amplifying circuit according to a first embodiment of the present invention.

Fig. 1 illustrates the major configuration of the dielectric line waveguide: Fig. 1A is a plan view illustrating the dielectric line waveguide from which an upper electrically conductive plate and an upper dielectric strip are removed; Fig. 1B is a sectional view of the dielectric line waveguide shown in Fig. 1A. In this embodiment, as illustrated in Fig. 1B, two electrically conductive plates 1 and 2, which form two plane parallel conductors, are grooved. Then, dielectric strips 3a and 3b are fit into the respective grooves, and a dielectric plate 4 is inserted between the dielectric strips 3a and 3b. An NRD guide (hereinafter simply referred to as a "dielectric line waveguide") is thus constructed. Formed on the upper surface of the dielectric plate 4 are, as shown in Fig. 1A, ground conductors 5a and 5b having a width W which equals an amount required for blocking an RF signal propagating in the dielectric line waveguide. For example, the width of the ground conductors 5a and 5b should be 1 mm or longer in a 60 GHz-band dielectric line waveguide. A slot line 6 is interposed between the opposing ground conductors 5a and 5b in a direction along the center axis of the dielectric strips 3a and 3b. The width of the slot line 6 is determined by the required characteristic impedance of a dielectric line waveguide to be designed. For example, a slot line 6 having a width of 0.05 to 0.5 mm makes it possible to obtain the characteristic impedance having 120 to 300 Ω of a resulting dielectric line waveguide. Disposed at both sides of the respective ends of the slot line 6 are line-switching conductor patterns 7a, 7b, 8a and 8b, which serve as connecting portions for smoothly guiding a signal propagating in the dielectric strips 3a and 3b to the slot line 6, and which are coupled to electromagnetic fields generated in the dielectric strips 3a and 3b of the dielectric line waveguide and electromagnetic fields generated in the slot line 6. In this embodiment, the line-switching conductor patterns 7a through 8b are formed in the shape of a dipole antenna. In order to reduce line-switching losses by lowering the wiring resistance of the line-switching conductor patterns 7a through 8b, the joint portions of the conductive patterns 7a through 8b with the ground conductors 5a and 5b are formed to be gradually narrowed, as indicated by R in Fig. 1A, as they advance from the ground conductors 5a and 5b to the conductor patterns 7a through 8b. Reference numeral 11 indicates a field-effect transistor (FET) which is mounted at the center of the slot line 6 in such a manner that it bridges over the slot line 6. Notched patterns having a predetermined length in a direction perpendicular to the slot line 6 are formed between the FET 11 and the conductor patterns 7a and 8b, respectively, so as to

form $\lambda/4$ short stubs 14 and 15. The $\lambda/4$ short stubs 14 and 15 serve to provide impedance matching between FET 11 and the line-switching conductor patterns 7a and 8b, respectively. Moreover, a gate terminal 12 and a drain terminal 13 are withdrawn to the exterior of the dielectric strips 3a and 3b from the position at which the FET's terminals are connected.

Fig. 2 illustrates the configuration of the FET 11 shown in Fig. 1 and its mounting area: Fig. 2A is a plan view of the FET 11; and Fig. 2B is a plan view of the dielectric plate 4 on which the FET 11 is mounted. The FET 11 has, as shown in Fig. 2A, active layers 25 and 26 where metal semiconductor field-effect transistors (MES-FET) are formed, and source terminals 21 and 22, a gate terminal 23, and a drain terminal 24 are withdrawn from the MES-FETs. Cross-hatching portions shown in Fig. 2A designate via-holes through which the respective terminals are led to the reverse surface of the chip. Reference numerals 16 and 17 shown in Fig. 2B respectively indicate a gate connecting conductor and a drain connecting conductor, both of which are used to branch the slot line 6, formed between the ground conductors 5a and 5b, into two portions, and also to couple the gate terminal 23 and the drain terminal 24, respectively, with the slot line 6. A gate bias voltage and a drain voltage are respectively applied to the gate terminal 12 and the drain terminal 13 on the dielectric plate 4 shown in Fig. 1A, so that the FET 11 forms a complementary amplifying circuit. The arrows shown in Fig. 2B designate the electromagnetic-field distribution of a signal propagating in the slot line 6. A longitudinal section magnetic (LSM)-mode signal, which propagates in the dielectric line waveguide in a direction from upward to downward as viewed from Fig. 2, is converted into a transverse electric (TE)-mode signal in the line-switching conductor patterns 7a and 7b shown in Fig. 1. The TE-mode signal further travels in the slot line 6 and is applied as a voltage signal between the gate terminal 23 and the source terminals 21 and 22 of the FET 11. Then, the TE-mode source-drain voltage signal again propagates in the slot line 6, and is converted into an LSM-mode voltage signal in the line-switching conductor patterns 8a and 8b. The converted LSM-mode signal further propagates in the dielectric line waveguide.

Fig. 3 illustrates another configuration of the line-switching conductor patterns 7a and 7b. In the example shown in Fig. 3A, $\lambda/4$ -length slot lines 9a and 9b having different widths are respectively formed between both sides of the end of the slot line 6 and the line-switching conductor patterns 7a and 7b. The slot lines 9a and 9b respectively serve to eliminate the generation of reflection between the conductor patterns 7a and 7b and the slot line 6, and also to provide impedance matching between the slot line 6 and the dielectric line waveguide and between the slot line 6 and the conductor patterns 7a and 7b. Further, in the example shown in Fig. 3B, the widths of the slot lines 9a and 9b having a $\lambda/2$ length or longer are gradually changed to provide impedance

matching between the slot line 6 and the dielectric line waveguide and between the slot line 6 and the conductor patterns 7a and 7b.

An explanation will now be given with reference to Fig. 4 of the configuration of a dielectric line waveguide provided with a frequency variable portion of a voltage-controlled oscillator (VCO) according to a second embodiment of the present invention.

Fig. 4A is a plan view of a dielectric line waveguide from which an upper electrically conductive plate and an upper dielectric strip are removed; Fig. 4B is a sectional view of the dielectric line waveguide shown in Fig. 4A. In the second embodiment, as well as in the first embodiment, two electrically conductive plates 1 and 2, which form two plane parallel conductors, are grooved, as illustrated in Fig. 4B. Then, dielectric strips 3a and 3b are fit into the respective grooves, and a dielectric plate 4 is inserted between the dielectric strips 3a and 3b. A dielectric line waveguide is thus constructed. Formed on the upper surface of the dielectric plate 4 are, as shown in Fig. 4A, ground conductors 5a and 5b having a width which equals an amount required for blocking an RF signal propagating in the dielectric line waveguide. A slot line 6 is formed between the opposing ground conductors 5a and 5b in a direction along the center axis of the dielectric strips 3a and 3b. Disposed at both sides of one end of the slot line 6 are line-switching conductor patterns 7a and 7b, which serve as connecting portions for smoothly guiding a signal propagating in the dielectric strips 3a and 3b to the slot line 6, and which are coupled to electromagnetic fields generated in the dielectric strips 3a and 3b of the dielectric line waveguide and electromagnetic fields generated in the slot line 6. A variable-capacitance diode 31 is mounted on the slot line 6 in such a manner that it bridges over the slot line 6. With this arrangement, a signal, which propagates in the dielectric line waveguide in a direction from downward to upward as viewed from Fig. 4, is coupled to the conductor patterns 7a and 7b and further propagates in the slot line 6. The capacitance of the variable-capacitance diode 31 is changed by a control voltage applied between the ground conductors 5a and 5b. Moreover, a terminating device 32 is mounted rearward (upward in Fig. 4A) of the diode 31, and a DC-blocking circuit 33 formed in a meandering shape is further disposed at the rear of the terminating device 32 so as to narrow the slot width between the ground conductors 5a and 5b and lengthen the opposing distance therebetween. Accordingly, an RF signal propagating in the slot line 6 is terminated by the terminating device 32 and the DC-blocking circuit 33. Conversely, an RF signal propagating in the dielectric line waveguide is interrupted in the ground conductors 5a and 5b. The meandering DC-blocking circuit 33, which intimately couples with the dielectric line waveguide, effectively interrupts an RF signal propagating in the dielectric line waveguide. The DC-blocking circuit 33 may be combined with an oscillator circuit to construct voltage-controlled oscillator circuitry. To

achieve this modification, the following configuration of an oscillator circuit may be considered by way of example. In a manner similar to the dielectric line waveguide shown in Fig. 4A, ground conductors and a slot line are disposed on the upper surface of a dielectric plate, and line-switching conductor patterns, which are coupled with electromagnetic fields generated in the dielectric strips of the dielectric line waveguide and electromagnetic fields generated in the slot line, are formed at both sides of one end of the slot line. Further, an oscillation diode is mounted on the slot line in such a manner that it bridges over the slot line.

In this manner, the mode of the dielectric line waveguide having a comparatively high characteristic impedance is converted into a mode of the slot line having a characteristic impedance (100 to 200 Ω) which is akin to the impedance of a variable-capacitance diode. This increases the impedance-variable range of the variable-capacitance diode 31, thereby widening the frequency-variable range.

Although in the embodiment shown in Fig. 4 both of the terminating device 32 and the DC-blocking circuit 33 are disposed, only one of the elements may be sufficiently provided.

The configuration of a dielectric line waveguide including a mixer circuit according to a third embodiment of the present invention will now be described while referring to Figs. 5 through 7.

Fig. 5A is a plan view of a dielectric line waveguide from which an upper conductor plate and an upper electrically dielectric strip are removed; and Fig. 5B is a sectional view of the dielectric line waveguide shown in Fig. 5A. The third embodiment is similar to the first embodiment in the following configuration of a dielectric line waveguide. Two electrically conductive plates 1 and 2, which form plane parallel conductors, are grooved. Dielectric strips 3a and 3b are fit into the respective grooves, and a dielectric plate 4 is interposed between the dielectric strips 3a and 3b. Further, in a manner similar to the second embodiment, formed on the upper surface of the dielectric plate 4 are ground conductors 5a and 5b having a width which equals an amount required for interrupting an RF signal propagating in the dielectric line waveguide. A slot line 6 is interposed between the opposing ground conductors 5a and 5b in a direction along the center axis of the dielectric strips 3a and 3b. Moreover, disposed at the both sides of one end of the slot line 6 are line-switching conductor patterns 7a and 7b, which serve as connecting portions for smoothly guiding a signal propagating in the dielectric strips 3a and 3b to the slot line 6, and which are coupled to electromagnetic fields generated in the dielectric strips 3a and 3b of the dielectric line waveguide and electromagnetic fields generated in the slot line 6. Unlike the first and second embodiments, a mixer diode 34 is mounted on the slot line 6 in such a manner that it bridges over the slot line 6. An intermediate frequency (IF) terminal 35 is led from the position at which the

anode terminal of the mixer diode 34 is connected. The ground conductor 5a and the leading portion for connecting the mixer diode 34 and the IF terminal 35 form, not only a coplanar line, but also an RF choke 37.

Fig. 6 illustrates the configuration of the mixer diode 34 shown in Fig. 5. A Schottky-barrier junction layer 44 is formed under an anode electrode 41, and an anode terminal 38 and cathode terminals 39 are withdrawn from the Schottky-barrier junction layer 44. Moreover, capacitor electrodes 41' and 42 are provided to withdraw capacitive-coupling terminals 40. Cross-hatching portions shown in Fig. 6A represent via-holes through which the elements of the diode 34 are connected to the respective electrodes mounted on the dielectric plate 4 on the reverse surface of the chip.

Fig. 7 is a plan view illustrating part of the dielectric plate 4 on which the mixer diode 34 is mounted. The anode terminal 38 is connected to an IF terminal line 36; the capacitive-coupling terminals 40 are connected to the ground conductor 5a; and the cathode terminals 39 are coupled to the ground conductor 5b. Accordingly, a signal (a mixed signal of an RF signal and a local (LO) signal) propagating in the slot line 6 is applied between the anode and cathode electrodes of the mixer diode 34 via capacitance generated by the capacitor electrodes 41' and 42 so as to extract a $|f_{RF} - f_{LO}|$ IF signal from the IF terminal 35.

According to the above description, since the RF signal and the LO signal are frequency-converted within the dielectric line waveguide, conversion losses can be reduced. Moreover, since an IF signal is output from a coplanar line, connection with another microwave circuit can be easily performed.

In the foregoing embodiments, the line-switching conductor patterns formed in the shape of a dipole antenna are provided at both sides of at least one end of the slot line; however, a line-switching conductor pattern may be provided, as shown in Fig. 8, for a ground conductor located only one side of each end of the slot line. The example shown in Fig. 8 is a modification made to the dielectric line waveguide including an amplifying circuit stated in the first embodiment, and line-switching conductor patterns 7 and 8 are formed only on the side of the ground conductor 5b.

As is seen from the above description, the dielectric line waveguide of the present invention offers the following advantages.

A circuit formed of a semiconductor device is formed on the dielectric plate at a position corresponding to the inside of the dielectric strip. This eliminates the generation of parasitic coupling between the dielectric line waveguide and an external circuit, which would otherwise be caused if an external circuit is provided. Also, transmission losses generated at a connecting portion between the dielectric strip and the semiconductor device can be inhibited to a minimal level. Moreover, it is possible to fabricate the ground conductor and the line-switching conductor pattern on the dielectric plate

according to a technique similar to the typical manufacturing method for a printed wiring board. The manufacturing cost can thus be reduced.

Moreover, a frequency signal (RF signal) propagating in the dielectric line waveguide is interrupted in and by the action of the ground conductor disposed on the dielectric plate. Accordingly, two dielectric lines are formed in a continuous dielectric strip, and are connected to each other via the semiconductor device. It is thus possible to readily construct a dielectric line waveguide provided with an amplifying circuit by using, for example, a FET.

The impedance matching can be provided between the line-switching conductor pattern and the semiconductor device, thereby inhibiting transmission losses at a connecting portion between the slot line and the semiconductor device.

Further, the impedance matching can be provided between the slot line and the line-switching conductor pattern and between the slot line and the dielectric line waveguide. It is thus possible to suppress unwanted reflection, and inhibit transmission losses incident to a line-switching operation.

Claims

1. A dielectric line waveguide comprising:

two electrically conductive plates (1, 2) disposed substantially parallel to each other;
a dielectric strip (3a, 3b) disposed between said two electrically conductive plates (1, 2);
a dielectric plate (4) disposed between said two electrically conductive plates (1, 2);
a ground conductor (5a, 5b) formed on said dielectric plate (4) and having an area which equals an amount required for blocking a frequency signal propagating in said dielectric line waveguide, said ground conductor (5a, 5b) having a slot line (6) at a position corresponding to the inside of said dielectric strip (3a, 3b);
a line-switching conductor pattern (7a, 7b, 8a, 8b; 7, 8) provided for said ground conductor (5a, 5b) at a position corresponding to an end of said slot line (6), said conductor pattern (7a, 7b, 8a, 8b; 7, 8) being coupled to electromagnetic fields generated in said slot line (6) and in said dielectric strip (3a, 3b); and
a semiconductor device (11; 31; 34) disposed on said slot line (6) in such a manner that it bridges over said slot line (6).

2. A dielectric line waveguide according to claim 1, wherein said line-switching conductor patterns (7a, 7b, 8a, 8b) are respectively provided in positions at both sides of an end of said slot line (6), and wherein said semiconductor device (11; 31; 34) is disposed substantially at the center of said slot line

(6).

3. A dielectric line waveguide according to one of claims 1 and 2, wherein a $\lambda/4$ short stub (14, 15) used for providing impedance matching between said line-switching conductor pattern (7a, 8b) and said semiconductor (11) device is provided in a midpoint of said slot line (6).
4. A dielectric line waveguide according to one of claims 1 to 3, wherein an impedance matching (9a, 9b) circuit is provided between said line-switching conductor pattern (7a, 7b) and said slot line (6).

FIG.2 (A)

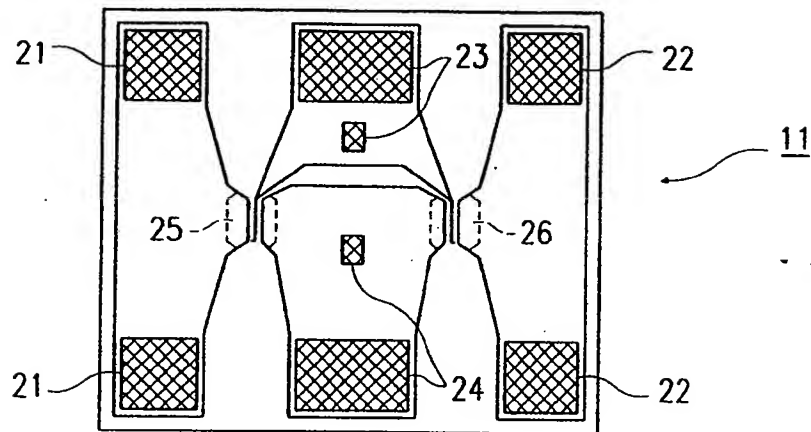


FIG.2 (B)

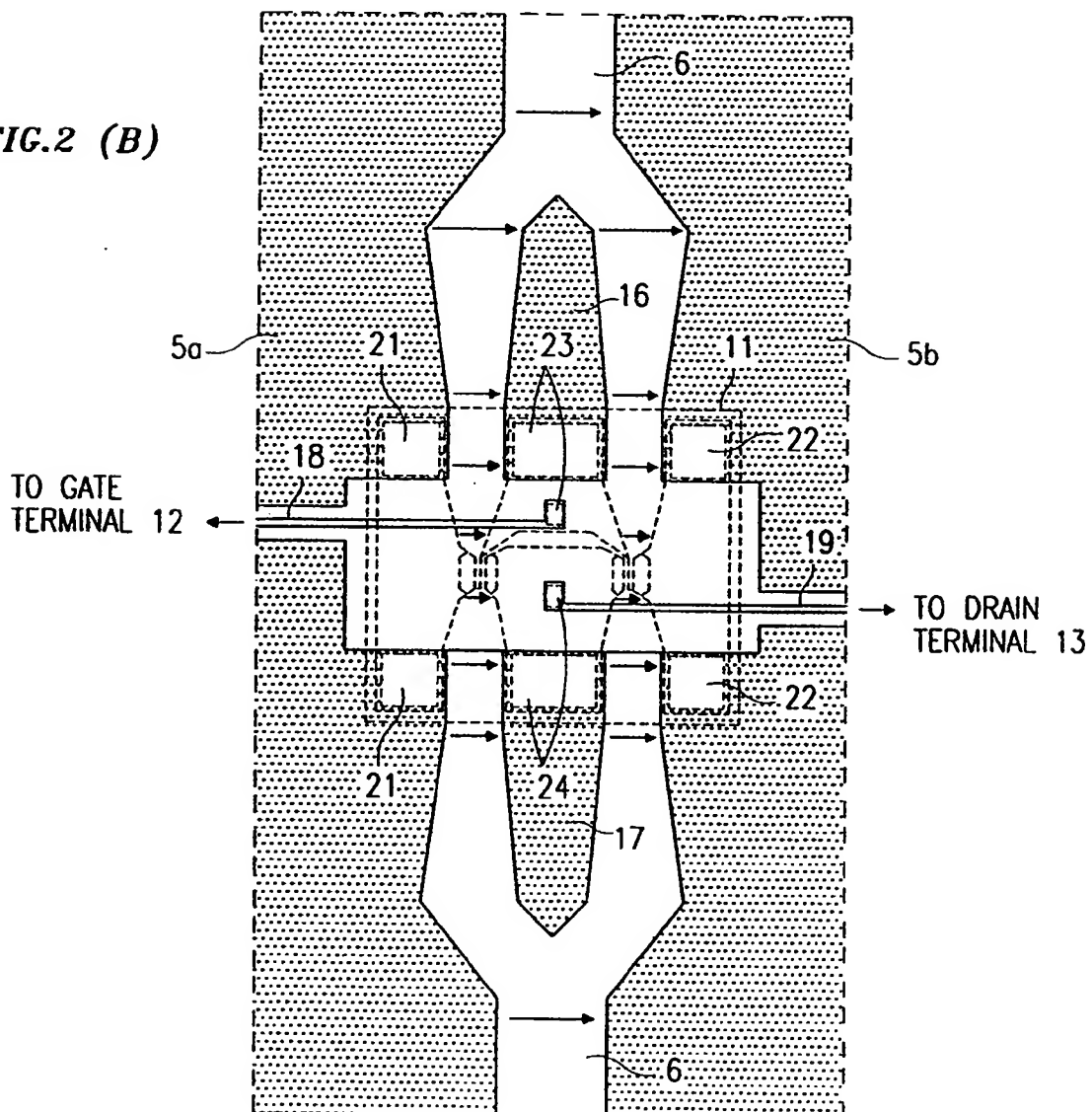


FIG. 3 (A)

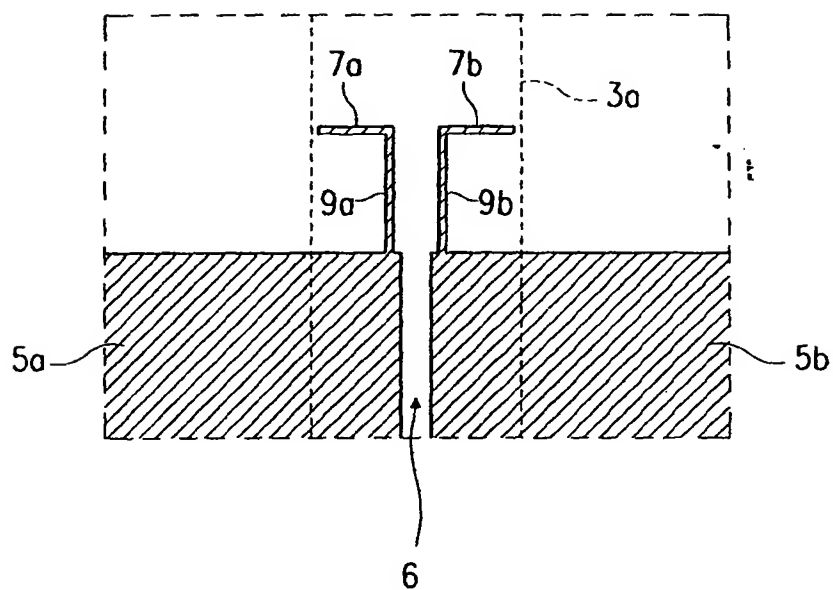


FIG. 3 (B)

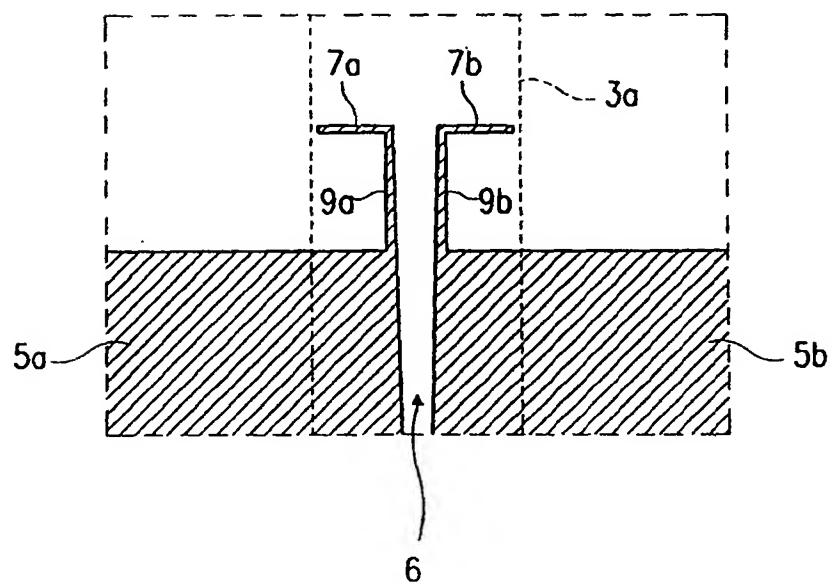


FIG. 4 (A)

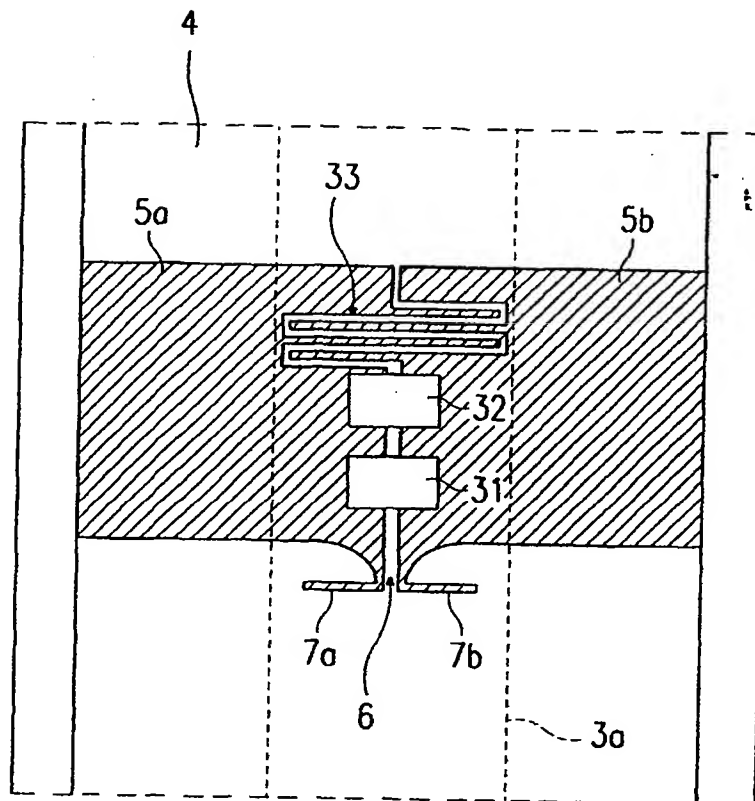


FIG. 4 (B)

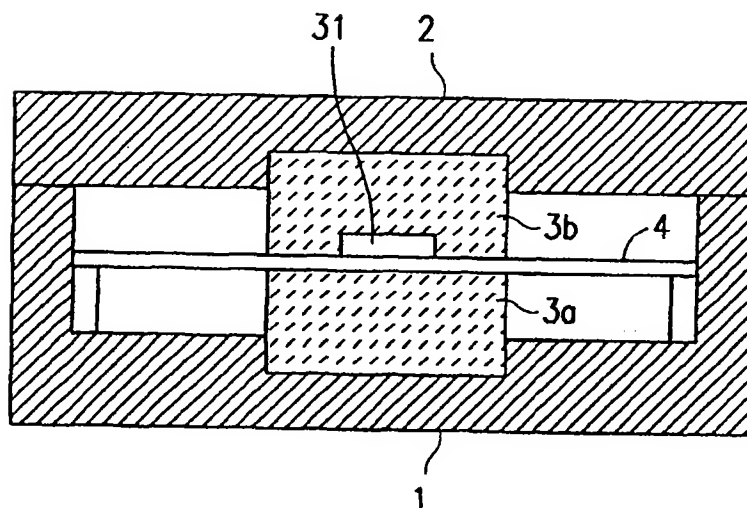


FIG.5 (A)

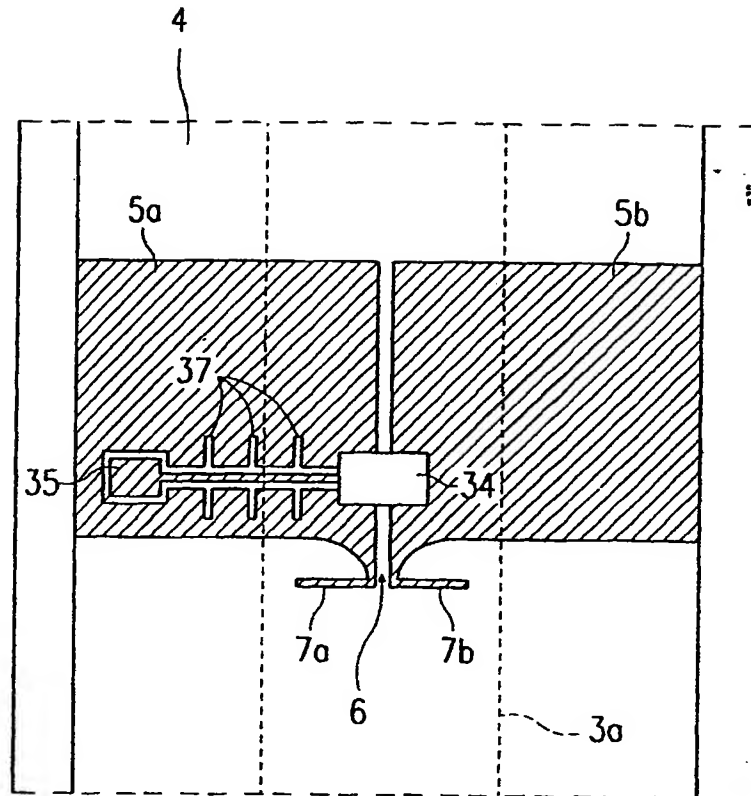


FIG.5 (B)

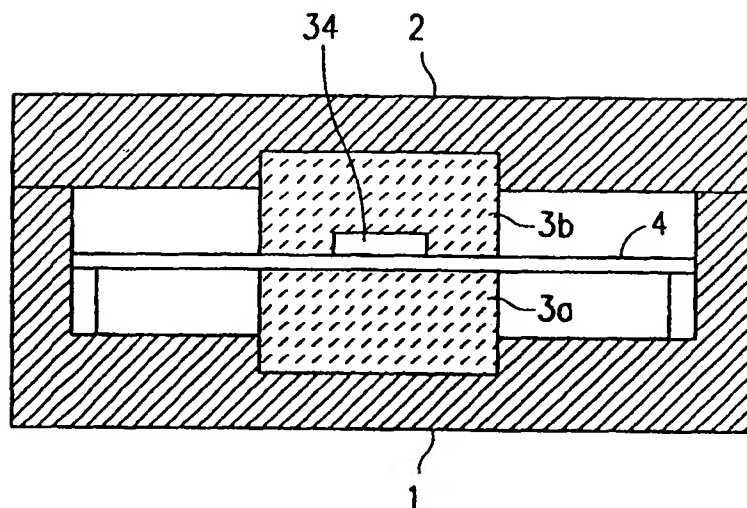


FIG. 6 (A)

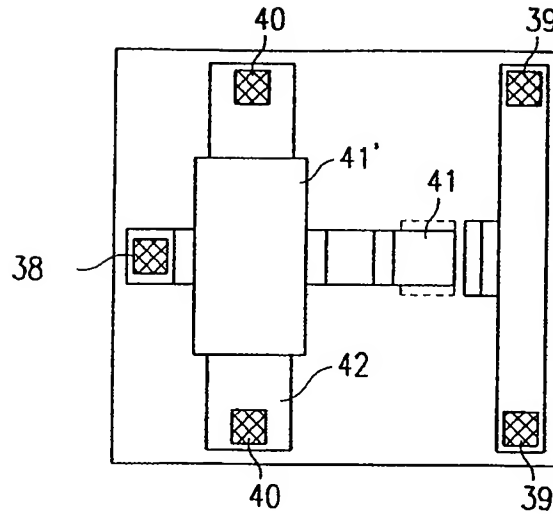


FIG. 6 (B)

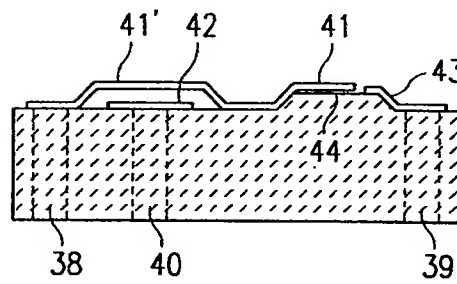


FIG. 7

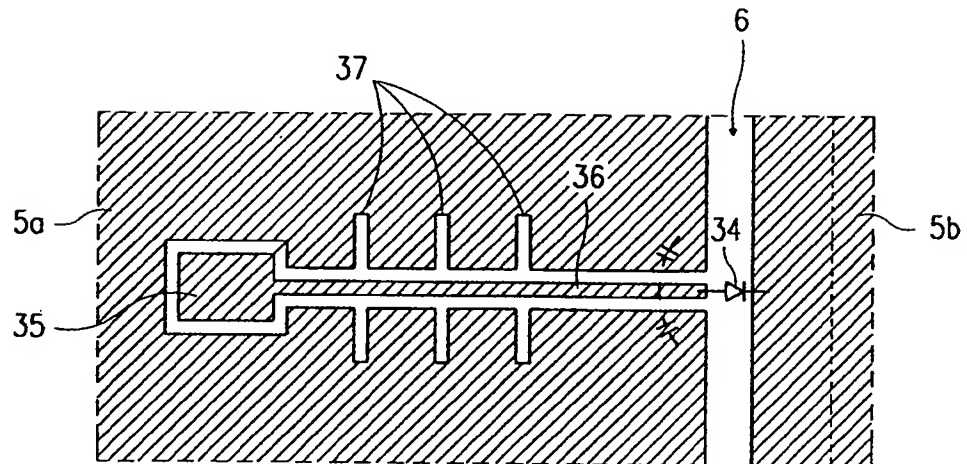


FIG.8 (A)

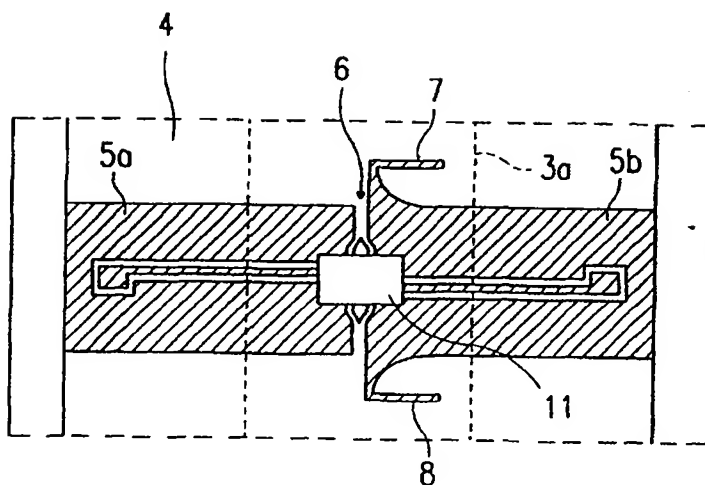


FIG.8 (B)

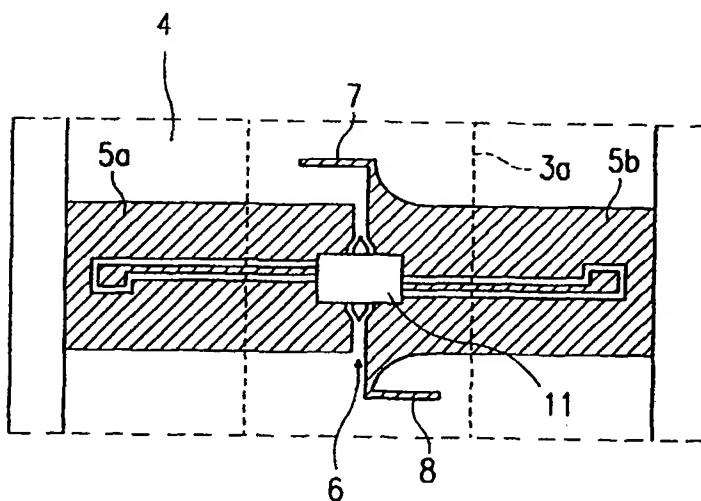
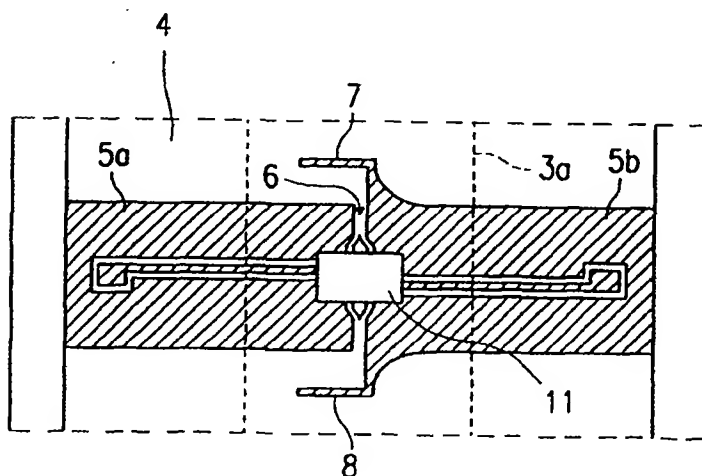


FIG.8 (C)





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 11 2280

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	ARTUZI W A ET AL: "A HEMT AMPLIFIER FOR NONRADIATIVE DIELECTRIC WAVEGUIDE INTEGRATED CIRCUITS" IEICE TRANSACTIONS, vol. E74, no. 5, 1 May 1991, pages 1185-1190, XP000258507 * page 1185, left-hand column, line 22 - page 1188, left-hand column, line 5; figures 1,2,4,5 *	1	H01P5/08
A	TSUKASA YONEYAMA: "MILLIMETER-WAVE INTEGRATED CIRCUITS USING NONRADIATIVE DIELECTRIC WAVEGUIDE" ELECTRONICS & COMMUNICATIONS IN JAPAN, PART II - ELECTRONICS, vol. 74, no. 2, 1 February 1991, pages 20-28, XP000240840 * page 24, right-hand column, line 18 - page 25, left-hand column, line 12; figure 13 *	1	
A	S.J. NIGHTINGALE ET AL.: "A 30 GHZ MONOLITHIC SINGLE-BALANCED MIXER WITH INTEGRATED DIPOLE RECEIVING ELEMENT" MICROWAVE JOURNAL., vol. 28, no. 8, August 1985, DEDHAM US, pages 103-116, XP002045046 * page 104, left-hand column, line 28 - middle column, line 6; figures 1,2 *	1	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01P H03D H03F
A	GB 1 438 149 A (NIPPON HOSO KYOKAI) * page 2, line 69 - line 122 * * page 4, line 15 - line 42; figures 1,12 *	1	
A	US 4 188 584 A (HOOGSTRAATE HENDRIK) * column 3, line 7 - column 4, line 24; figure 1 *	1	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 29 October 1997	Examiner Den Otter, A
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons</p> <p>& : member of the same patent family, corresponding document</p>			